Emission Microscope and Passive Voltage Contrast: Solving A Problem Quickly

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The SEM technique known as Voltage Contrast has a history going back more than 50 years. The Passive Voltage Contrast technique has been in use for only 6 years for detecting gate oxide breakdown in MOS devices.*

Voltage Contrast has wider applications, but can be used on semiconductor devices without deprocessing. Both e-beam probers and SEMs can use this technique to compare 5 V and 0 V signals. Passive Voltage Contrast (PVC) on the other hand is used to examine deprocessed devices in the passive state. In PVC, the electron beam of the SEM creates voltage contrast between areas in the contacts where electrons are being either charged or discharged. Areas of discharge, or areas with a path to ground, will appear bright, while charged areas of the contact will be dark.

Finding a defective transistor in an IC is like looking for a needle in a haystack. An emission microscope though, can lead the analysts to the approximate defective transistor. Combining these two techniques can solve a failure analysis problem quickly and elegantly.

The device in this case was a CMOS logic device with dual metallization which had failed in service. The description of the failure from the field pointed to a functional failure rather than a pin leakage failure. First, an emission microscope was used to find the approximate geographic location of the failure site. Next, the SEM PVC technique was used to examine and analyze the failure site.

The device was decapped and imaged first with the lowest power objective (0.8x) of a Hypervision Visionary 2000 emission microscope. Emission microscopes take advantage of the fact that most chip-level defects emit light. These defects include four types of leakage defects: saturation, avalanche, gate dielectric and forward biasing. The device was tested to replicate the failure experienced by the user. In this way, the defect at the failure site would emit light. The device is connected to an ATE equipment by a docking emission microscope, and test vectors from the ATE cause the functional defect to light up. The low power and very wide angle of this objective lens encompassed the whole area of the device (Figure 1).

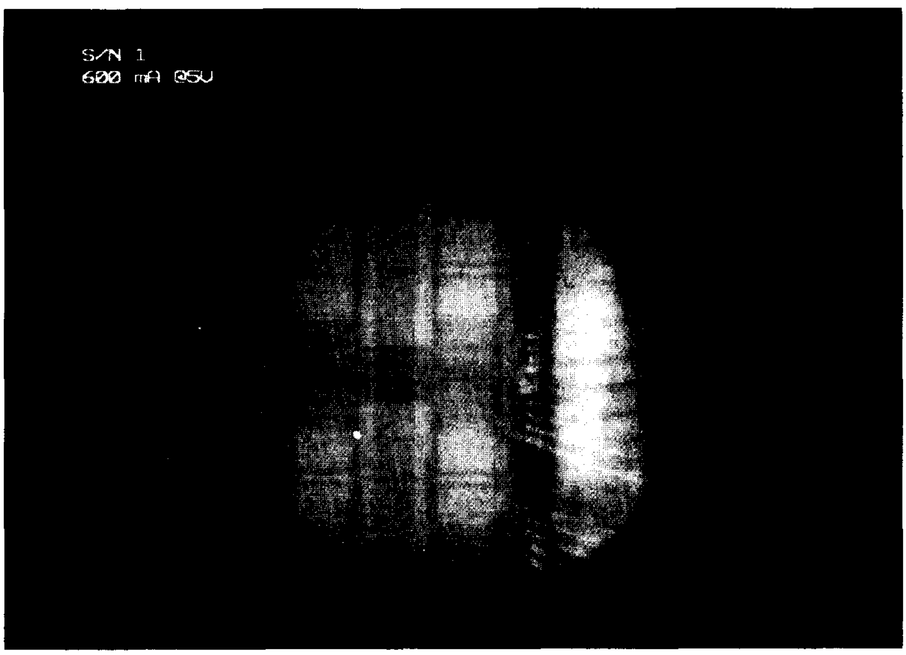

Figure 1. The emission site at low magnification.

Once the general location of the defect was known, successively higher magnifications were used to narrow down the defect site in the IC (Figure 2). The next step was to prepare the device for PVC Contrast imaging for any possible gate oxide breakdown. During the various stages of deprocessing all levels were visually checked for possible process

Figure 2. The emission site at high magnification.

defects around the emission site.

In preparation for PVC, classification was removed from the device with a plasma etch. Metal-2 and the intermetal oxide were then removed with phosphoric acid and hydrofluoric acid respectively. Finally, metal layer 1 was removed with phosphoric acid, and the metal-1 to poly and diffusion contacts were exposed. Deprocessing was stopped at the BPSG (BoroPhosphoSilicate Glass) level (Figure 3). Note that after removing the metal, poly gates will be floating. This is the right level for Passive Voltage Contrast regardless of how many metallization layers exist. The device was then mounted on a conductive sample holder, which is well grounded, and placed in the SEM (Hitachi 4200) chamber for PVC inspection.

To achieve the desired contrast, there are a few steps that must be followed. First, the substrate must be grounded by applying conductive carbon paint spread across it (Figure 4). The conductive carbon provides a path from the diffusion contacts to ground. Second, the PVC requires

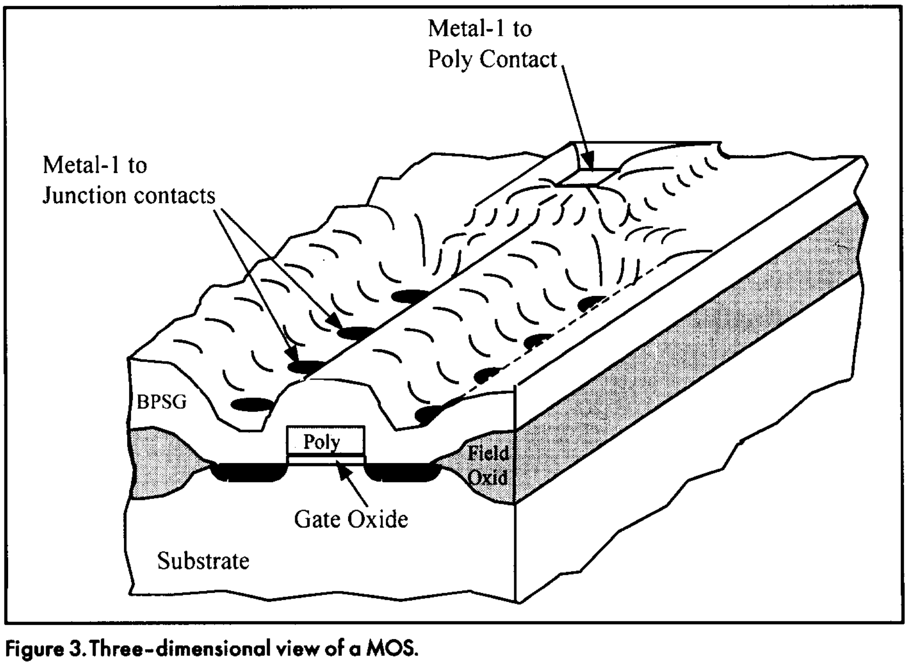

Figure 3. Three-dimensional view of a MOS.

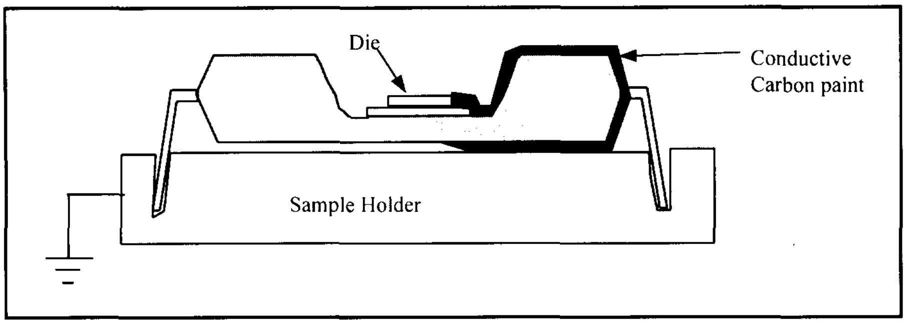

Figure 4. The cross section view of the sample preparation for the PVC in the SEM.

Figure 5a. Passive voltage contrast is showing the leaky poly.

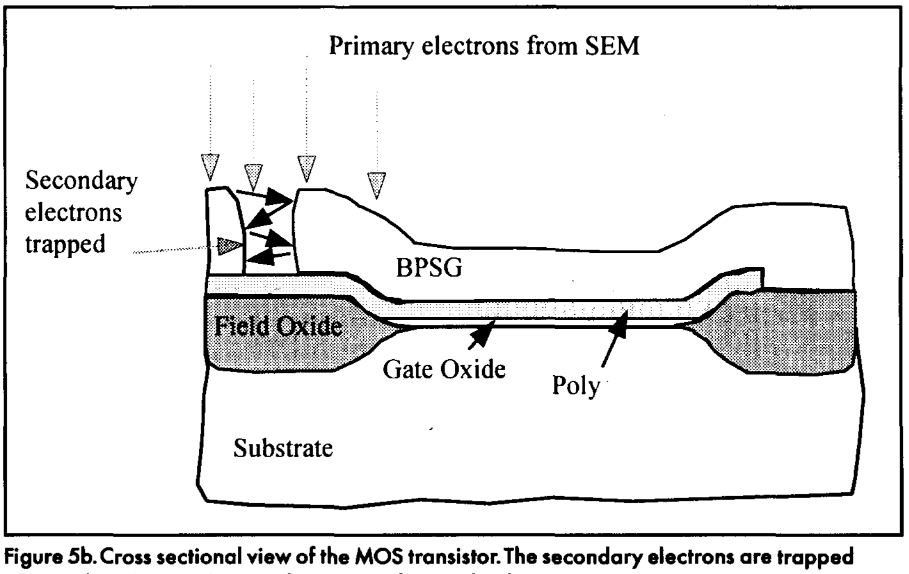

Figure 5b. Cross sectional view of the MOS transistor. The secondary electrons are trapped (charged) in the metal-1 to poly contact of a good poly gate.

proper tilt angle for the sample. In this case, the sample was tilted at 35 degrees. In other types of SEM work, tilting may not be important, but if a PVC sample is not tilted, all the contacts will charge up, and there may not be contrast between good and bad poly contacts. Tilting provides more secondary electrons. The result is increased secondary electron activity from grounded conductors (diffusion contacts). The diffusion contacts therefore appear bright, while non-conductors (poly contacts) should appear dark. Finally, the SEM accelerating beam voltage should be set at the lowest possible setting (i.e. 1 kV) because at high accelerating beam voltage, localized surface charging on the diffusion contacts will eliminate the desired contrast.

With follow-up inspection, the analyst should concentrate on looking at the poly contacts in the area where emission was observed. Since poly contacts are dark, if one contact is bright then this leads us to the defective poly or gate oxide (Figure 5). To confirm this poly contact's brightness, the analyst should zoom-in to the contact (7000x) and then zoom-out (800x). If the poly is not defective it builds-up charge at the contact and remains dark and if defective (shorted to substrate), the poly contact becomes bright.

Defects of this type usually appear as a spike from poly to substrate (Figure 6). The poly at the defective oxide will generate a high electric field during device operation. This will result in a penetration from poly through the gate oxide to the substrate causing an electrical short. Consequently every time that transistor is activated, it will be forward biased with the substrate (i.e. ground if NMOS). From this point on, further deprocessing is required to confirm the mechanism. In our case, the device was deprocessed down to substrate level using a diluted hydrofluoric acid. The defective area was then identified at high resolution in the SEM (Figure 7).

The combination of these two techniques, emission microscope and PVC, first identifies the location of the problem in a short period of time and second, eliminates the extensive and destructive work of using a mechanical prober.

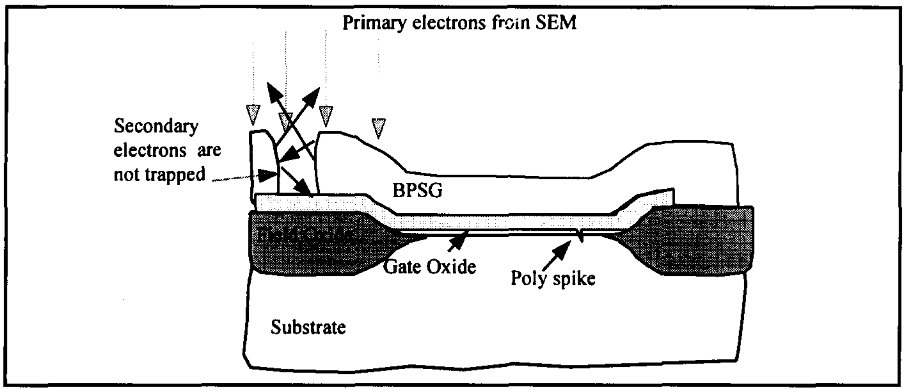

Figure 6: Cross sectional view of the MOS transistor with poly spike. Note that the electrons are not trapped in the contact.

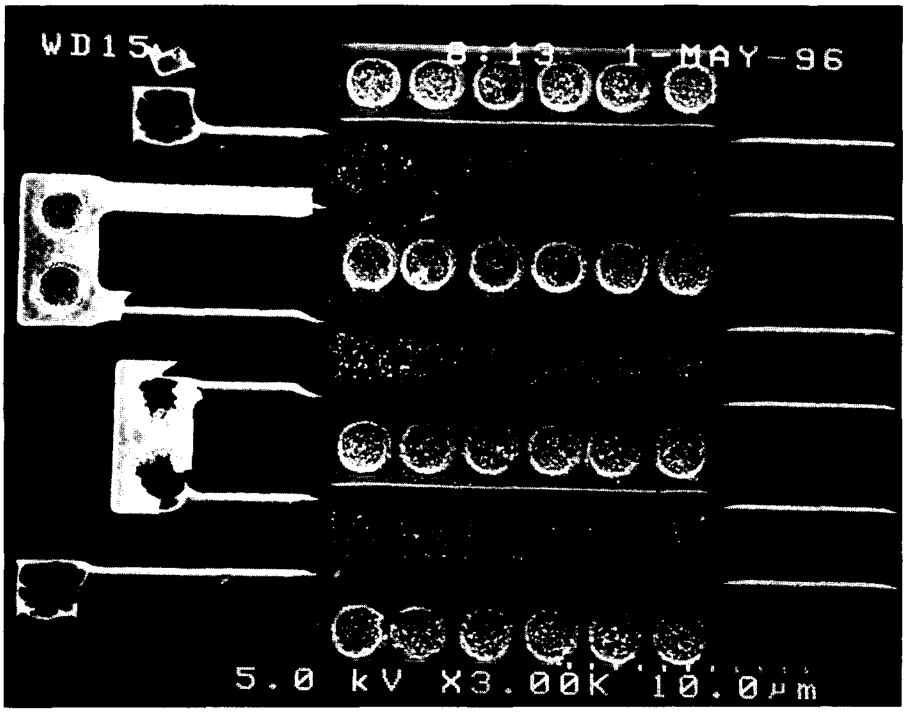

Figure 7a: The SEM picture at the silicon level shows the location of the gate oxide break down.

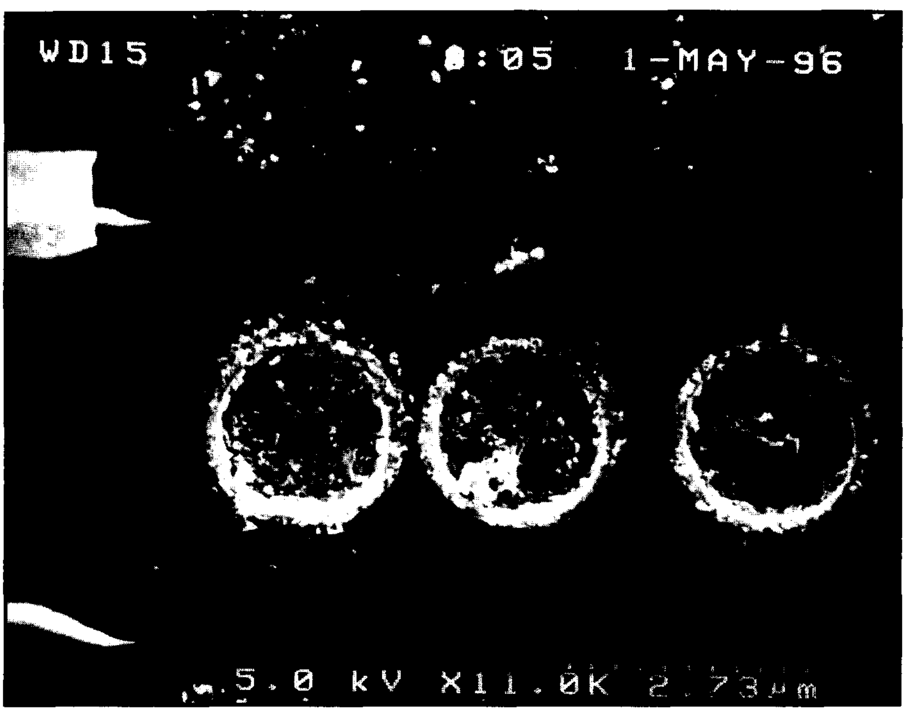

Figure 7b: Same as figure 7a at higher magnification.

*Reference

Colvin, Jim, "A new technique to rapidly identify gate oxide leakage in field effect semiconductors using a scanning electron microscope", ISTFA Symposium, 1990.

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